

PATENT
Attorney Docket No. 29610/CDT496

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:) For: Molecular Electronic Device
) Fabrication Methods and Structures
Julian Carter et al.)
) Group Art Unit: 1715
Serial No. 10/588,050)
) Examiner: James Lin
Filed: February 7, 2005 (Int'l. Appl.)
No. PCT/GB2005/000429) Confirmation No. 3599

**DECLARATION OF JULIAN CARTER, Ph.D.
PURSUANT TO 37 C.F.R. § 1.131**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Julian Carter, Ph.D., hereby states as follows:

1. I am a named co-inventor of the subject matter claimed in the above-identified patent application ("the application").
2. I make this declaration for the purpose of providing evidence that the methods of fabricating an organic light emitting diode device, as recited in the claims of the application, were reduced to practice before the September 9, 2003 filing date of U.S. Appl. Pub. 2005/0052120 to Gupta et al. ("Gupta") and subsequent to December 31, 1995.
3. Attached hereto as Attachments A and B are documents (or portions thereof) dated before September 9, 2003 and subsequent to December 31, 1995. Attachments A and B have been redacted to remove date information.
4. Attachment A is an internal research summary report entitled "Undercut bank process GOD11 single-colour displays for SID – ww19."
5. Attachment B includes the first three slides of a 34 slide internal research report entitled "GOD11 FIB Analysis – ww25 2003."

6. Attachments A and B and the organic light emitting diode devices described therein were prepared in Great Britain, which is a World Trade Organization (WTO) member country.

7. Attachments A and B have been maintained as business records in the normal course of business.

8. Attachment A describes the fabrication and performance of organic light emitting diode devices including an undercut bank consistent with the methods of fabricating an organic light emitting diode device claimed in the application. The fabrication and performance testing of the devices described in Attachment A were carried out either by me, by my co-inventors, under my direction and control, and/or under my co-inventors' direction and control.

9. The image of "CDT" shown in Attachment A is an actual image of a displayed message generated using an organic light emitting diode device including an undercut bank consistent with the methods of fabricating an organic light emitting diode device claimed in the application.

10. Attachment B also describes the fabrication and performance of organic light emitting diode devices including an undercut bank consistent with the methods of fabricating an organic light emitting diode device claimed in the application. The fabrication and performance testing of the devices described in Attachment B were carried out either by me, by my co-inventors, under my direction and control, and/or under my co-inventors' direction and control.

11. The SEM micrographs at pages 2 and 3 of Attachment B illustrate a cross-sectional view of an organic light emitting diode device including an undercut bank consistent with the methods of fabricating an organic light emitting diode device claimed in the application.

12. The banks of the devices described/illustrated in Attachments A and B were fabricated from a negative resist material in the ELX series (Zeon Corporation, Japan).

13. An organic hole transporting layer (PEDT) and an electroluminescent layer ("LEP") were "printed" (i.e., deposited by a droplet deposition technique) into wells defined by the banks in the devices described/illustrated in Attachments A and B.

14. In the illustrated pixel of the second slide of Attachment B, the height of the bank relative to the base of the well is approximately 0.6 μ m.

15. Attachments A and B demonstrate my co-inventors' and my successful reduction to practice of the methods of fabricating an organic light emitting diode device claimed in the application before the September 9, 2003 filing date of Gupta and subsequent to December 31, 1995. Furthermore, Attachments A and B demonstrate my co-inventors' and my successful possession of and at least as much as is shown in Gupta before the September 9, 2003 filing date of Gupta and subsequent to December 31, 1995.

16. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001 and that such willful false statements may jeopardize the validity of the above-referenced patent application and any patent issued therefrom.

Dated: 2nd March 2012



Julian Carter, Ph.D.

From: Haydn Gregory
Sent:
To: Disco Project; Matthew Davison
Subject: Undercut bank process GOD11 single-colour displays for SID - ww19

Undercut bank process GOD11 single-colour displays for SID - ww19

Background

Following the previous apparent success with using thinned Zeon ELX material as the bank, both 14" and 6" undercut bank substrates were prepared with cathode separator by SPG and then printed and processed into displays to try and yield something ready for SID 2002 (ww21).

Results

Initial substrates

Six 14" substrates were processed in two sessions, together with four 6" substrates through the Cambridge route, over a week or so. It was clear that there was some variation in results for these early substrates, and there was a scattering of dead pixels over most displays together with non-lighting rows:

The peppering of bad pixels usually seemed to be at the edges of the displays, but often had the distinct appearance of being a streak across the display.

Subsequent substrates

The later batch of substrates, printed as 6", showed a dramatic reduction in the number of dead pixels i.e. the spottiness had fundamentally disappeared:

Here are a couple of "real" pulse-driven images on the best of the current process displays:

The dead rows were still there though, and was shown to be linked to a high impedance in the continuity between anode metal and cathode metal i.e. probably at the bank contact window. This was backed up by examining both the continuity structures in each display (single cathode-separated cathode metal stripe over flat vs. pixel bank topography), and some of the cathode serpentine test cell structures (serpentine cathode metal over glass vs. over bank edges).

Row failures

The previous WIX bank process - which had a shallow edge slope of 15-20degrees - exhibited a delta between the two display continuity stripes of ~10 Ohms, and a difference in cathode serpentine resistance of ~2 Ohms. The current ELX bank process, however, showed a best case stripe continuity delta of ~30 Ohms - with large variation up to open-circuit - and a typical serpentine continuity delta of megaOhms i.e. the cathode generally became open-circuit running over bank topography.

This indicates that the edges of the bank are actually separating the cathode along a row, and that the main contact window in the bank between anode metal to cathode is often becoming

open-circuit. This is probably either due to excessive undercut in the bank edge, or the bank layer being too thick &/or cathode Al layer being too thin to conform to the steep edge of the bank. There will obviously be an optimum "sweet spot" for this bank profile - needing to balance ink wetting and cathode continuity over the back of the pixels - and currently it is too far in the favour of breaking the cathode over the undercut bank edge.

Even though there are generally only a handful of missing rows per display, the resistance of the cathode layer in a functioning display row is actually currently very high i.e. it's on the edge of being a functioning process. This was evident by sometimes seeing a decrease in pixel emission as you move down the row away from the contact window, and was confirmed by micro-probing down onto the cathode row stripe on the back of the pixels and getting very high impedance between adjacent pixels. One would expect fractions of Ohms, but instead see megaOhms in a lot of cases. Note, it was often seen that the dead rows all occurred for the cathode stripes connected at one particular side of the display (the odd & even rows are connected from left & right respectively), but there's been no clear systematic reason found for this handedness yet.

Conclusions

Two good displays were produced for SID 2002, and two obvious failure modes have been identified with the undercut bank process. This is a good improvement over the slopey WIX bank process, and gives a base for the further process development and ink transfer to the pilot line.

Future Work

* The ELX undercut bank profile (together maybe with cathode thickness tweaks) needs to be brought into a non-sensitive process regime, so that the cathode continuity delta is consistently low and row failures do not occur i.e. so the cathode never starts to break over the bank edges (some thinning is always likely to occur). It may be that the optimum bank edge profile is when it is positive at 60degrees or so - in line with the PEDT-on-bank contact angle.

* Investigate any remnants of the spotty pixel failures the gross effect was hopefully due to poor substrate cleanliness seen for the early stages process development only and won't recur seriously again.

* Edit print recipes to stop overprinting onto the test cells, to allow routine measurement of the cathode serpentine structures & the specific Kelvin contact resistance.

Regards,
Haydn

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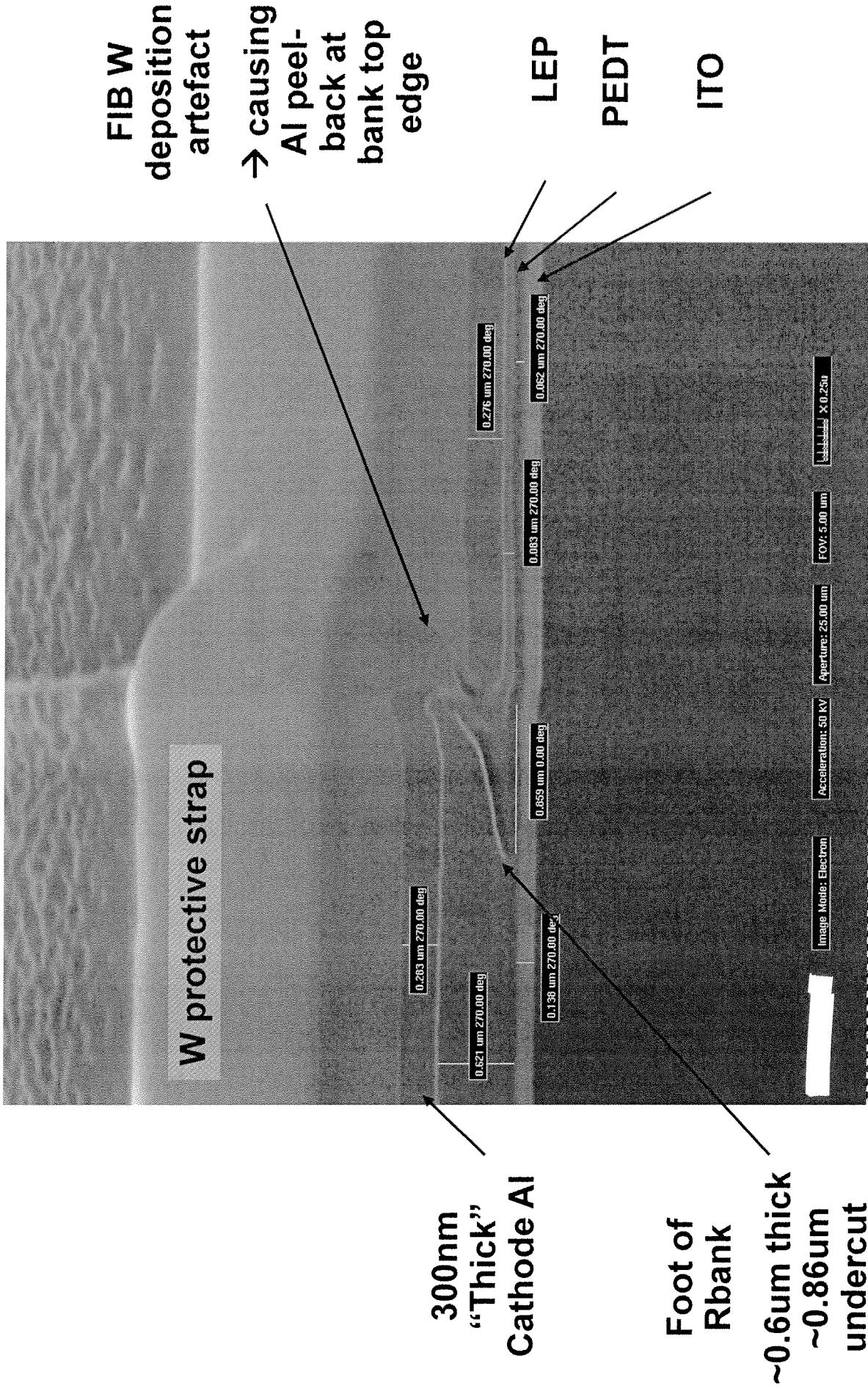
0.60um Rbank, 120s PEB, 300nm Al C2 (Good pixels & rows, but spotty)

- 0231-02 c36, Row33 Col95 Pixel
 - Large undercut Rbank structure ~0.86um, with “horn” shape to it
 - PEDT fills undercut
 - LEP runs up PEDT side-wall to tip of Rbank, creating near-vertical wall
 - Cathode Al appears to break sometimes over Rbank edge
 - this appears to be accentuated by the FIB W strap process
 - Large Cathode Separator undercut ~1.24um
 - Thinner layer than expected at ~2.6um
 - . Some evidence of undercut asymmetry ~0.07um
 - . Good cathode separation, with ~0.5um under-hang
 - . Some evidence of cathode under-hang asymmetry ~0.11um;
 - . Some evidence from shadowing effect even though substrate is rotated during evaporation (note, this sample was on the lower RHS substrate edge)
 - Dead pixels are clearly imaged by FIB as dark pixels when caused by discontinuous cathode Al over Rbank edges;
this is because where there is no imaging current flow (to earth straps placed across display metalisation) it appears dark
 - Good cathode separation is also clearly imaged as a dark feature, and the not-completely separating separators appear bright
 - Poorly connecting row contact windows causing dead rows also appear dark by FIB
 - A number of problems were found here, with discontinuity of Al seen over both AM & Rbank edges
 - The current flow for some rows is clearly only through the outer edge of the window i.e. the current has to double-back on itself
 - Likely ballooning of the Rbank away from AM i.e. CDs change significantly over AM or mask diffraction effect

CDT

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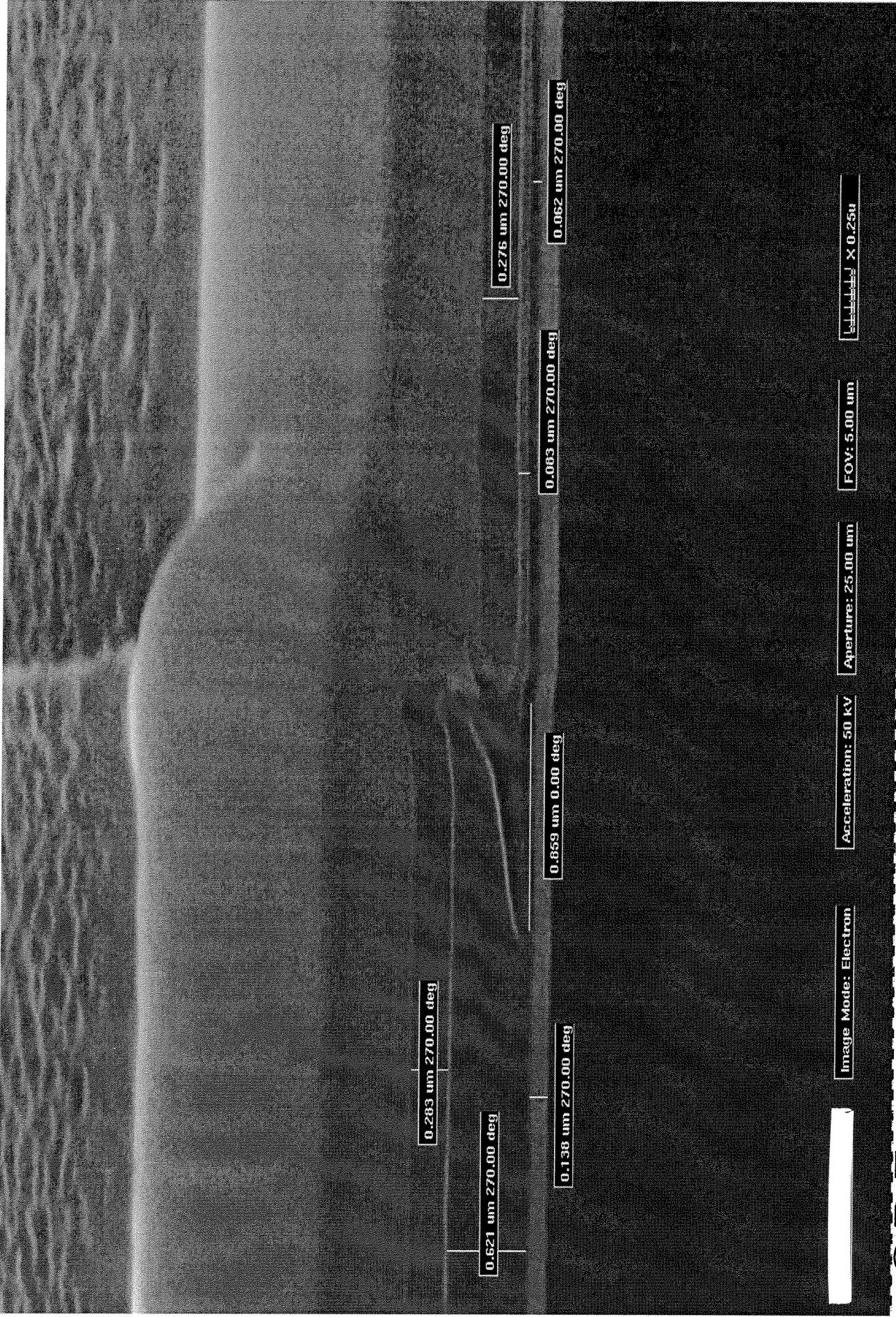
0.60um Rbank, 120s PEB, 300nm Al C2 – Bank Cross-sectional FIB Profile



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0.60um Rbank, 120s PEB, 300nm Al C2 – Bank Cross-sectional FIB Profile



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